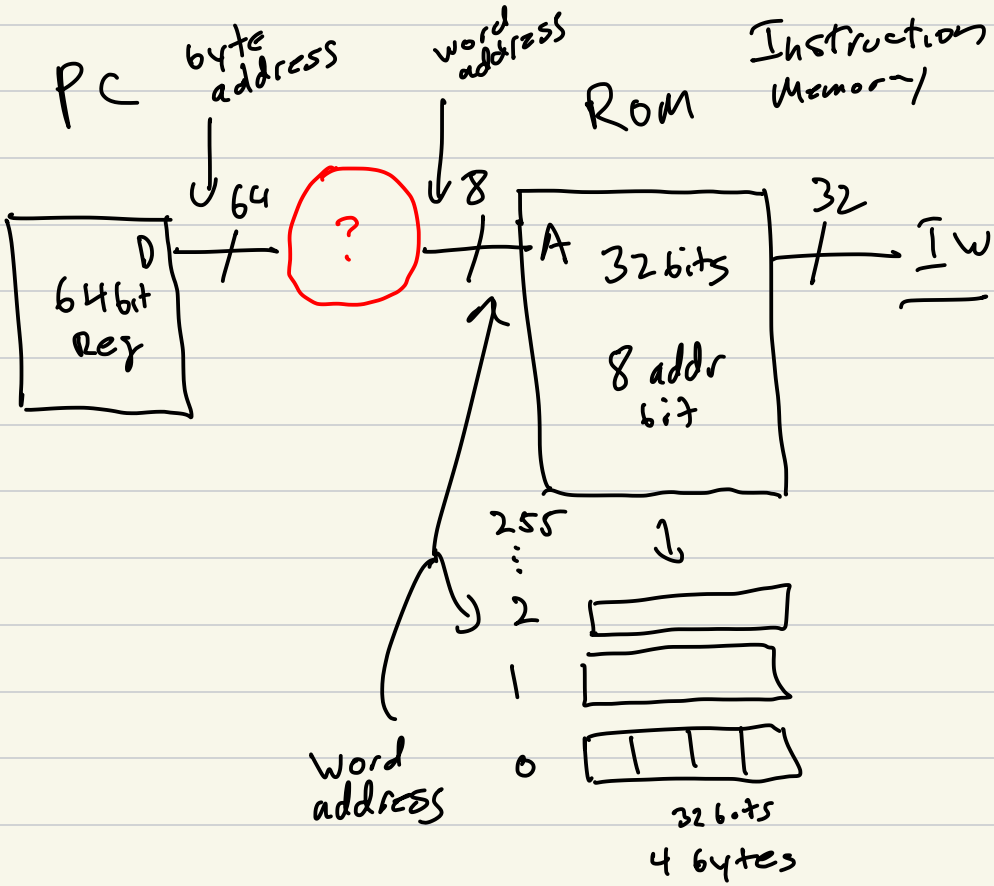
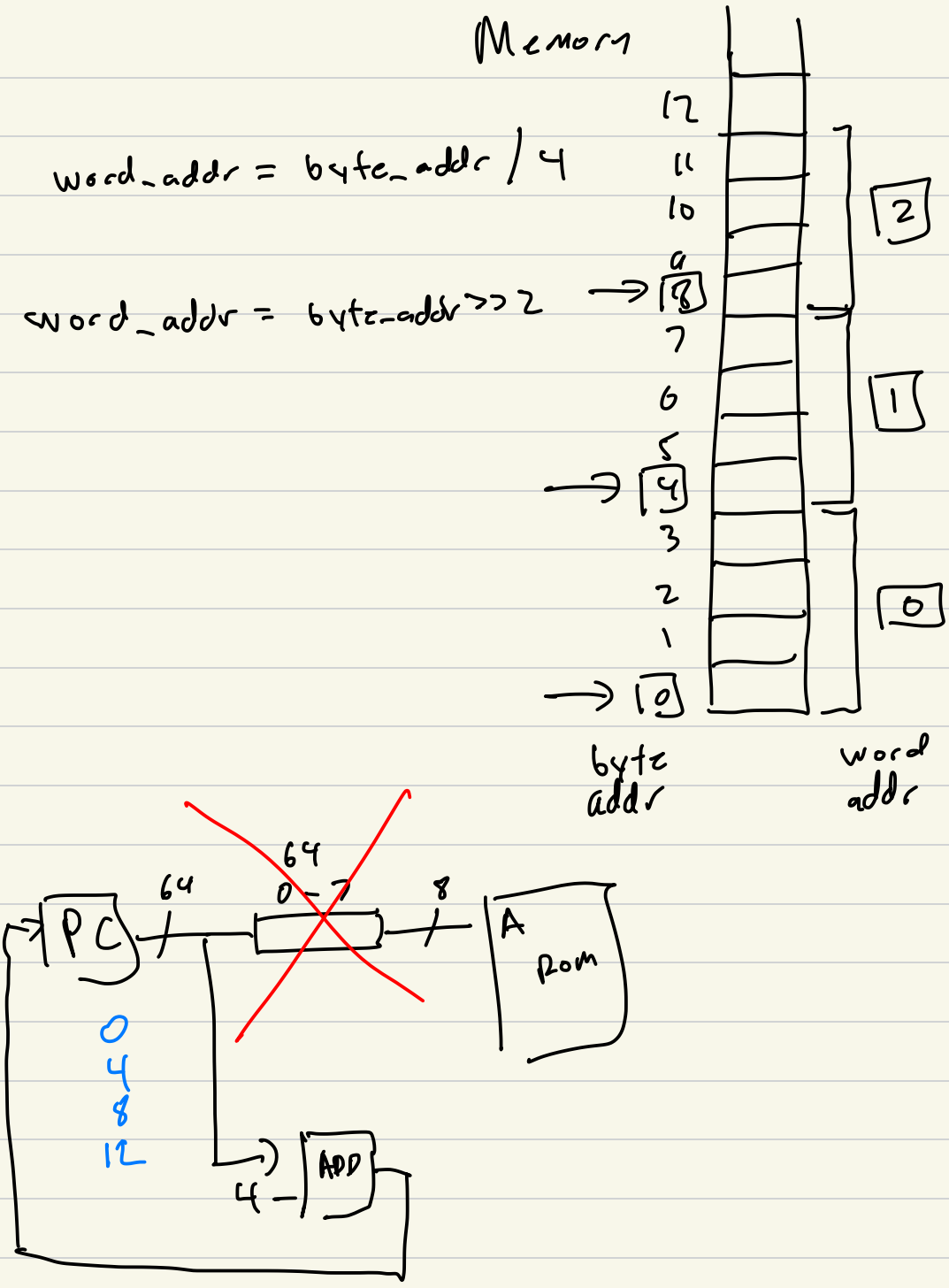
CS315-01 Processor Decoding

Lab05 - RegFile, ALU

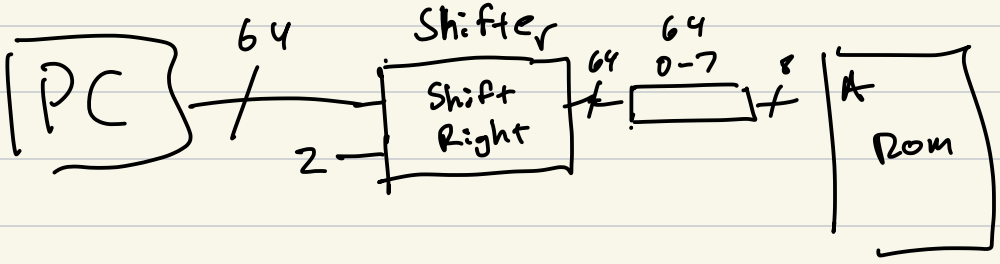


8 bit addr means the ROM can hold $2^8 = 256$ instruction words

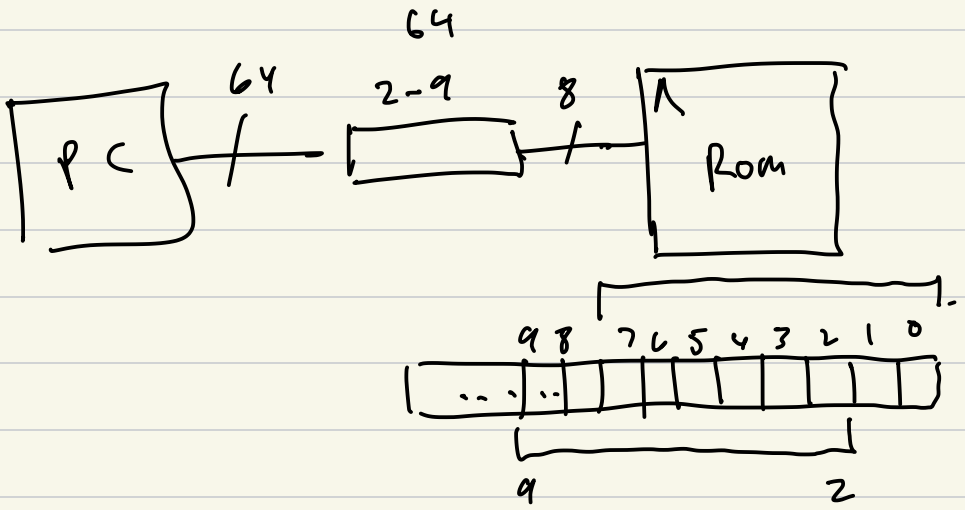

Memory
word_addr = byte_addr / 4
word_addr = byte_addr >> 2
12
11
10
9
8
7
6
5
4
3
2
1
0
2
1
0
byte addr
word addr
64
0 - 7
8
PC
64
A
Rom
0
4
8
12
4
ADD

byte addr to word addr

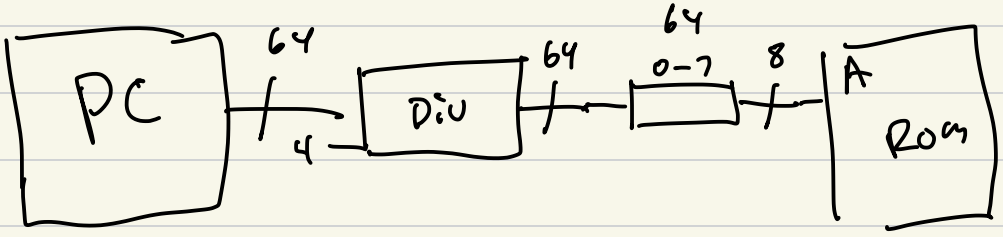
①

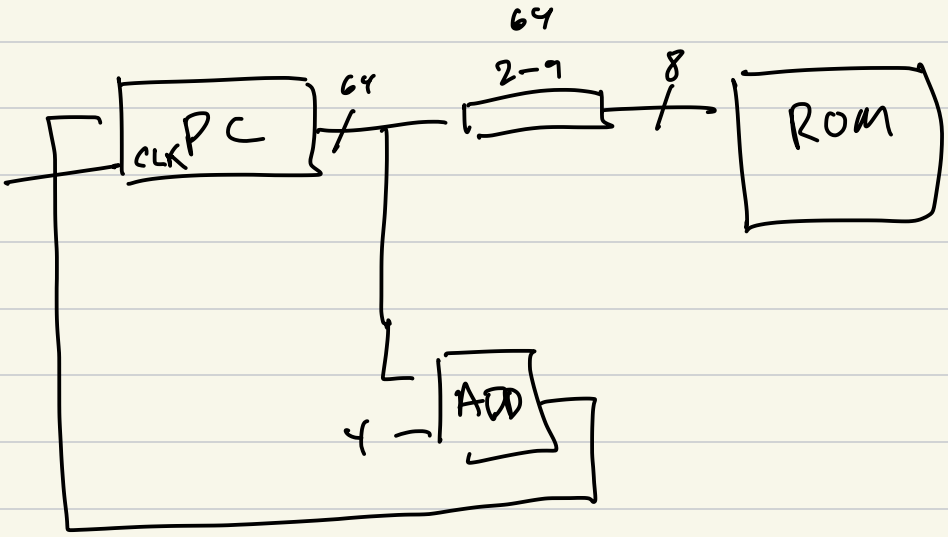


②

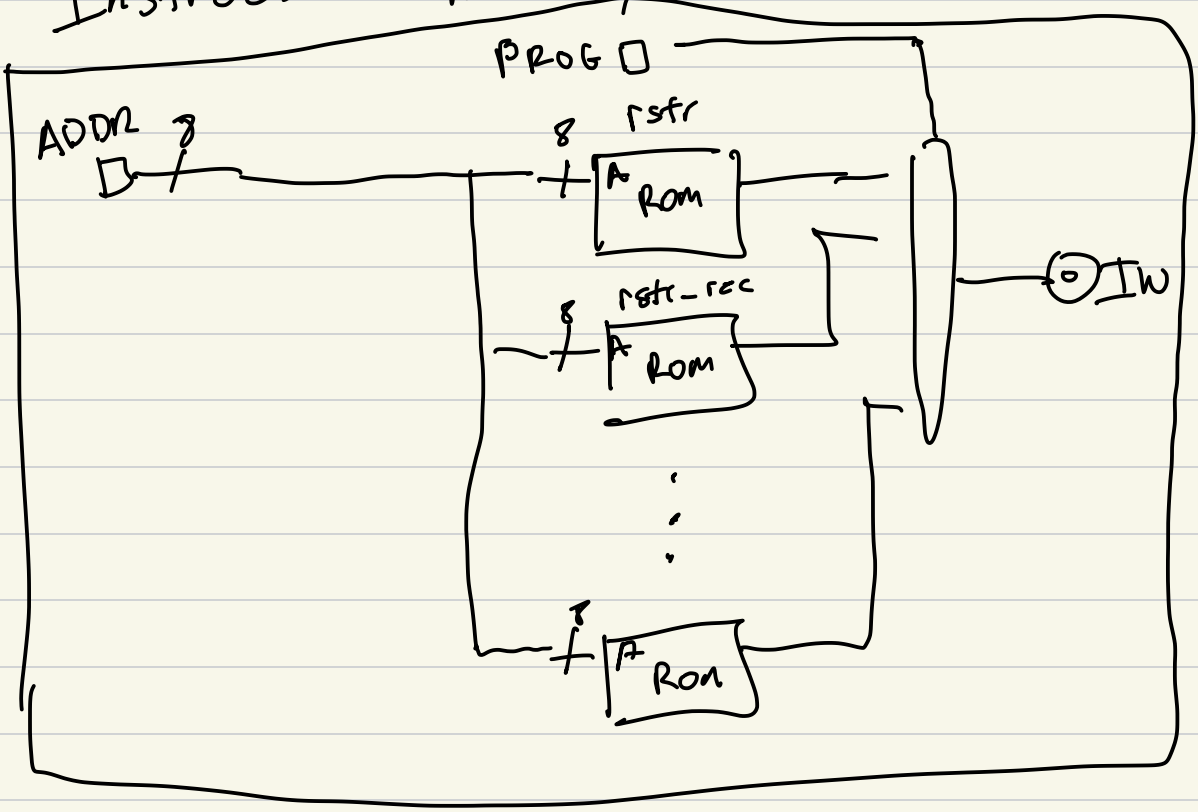


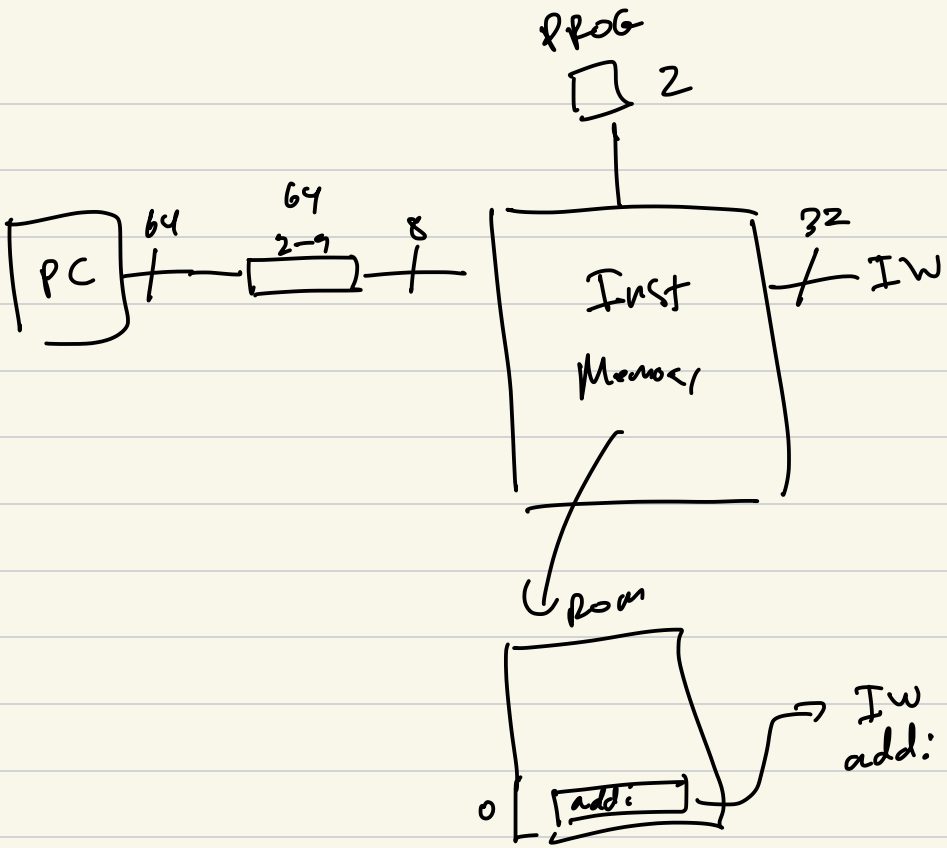
③



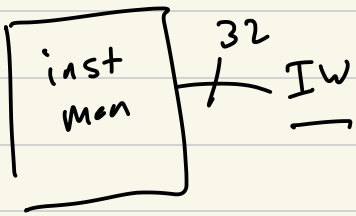


Instruction Memory





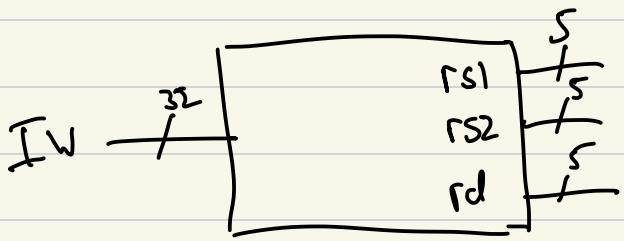
IW instruction word



Decoding

RegDecoder
ImmDecoder
InstDecoder

RegDecoder



=> RegFile

one splitter

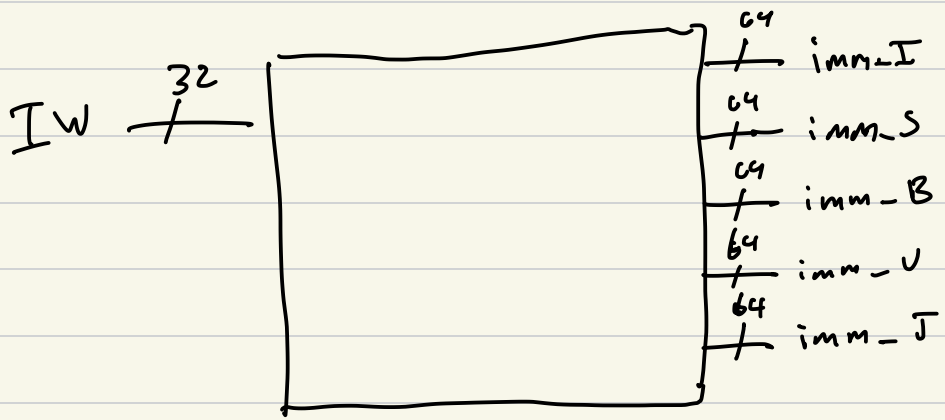
add t0, t1, t2

rs1 rs2

6 7

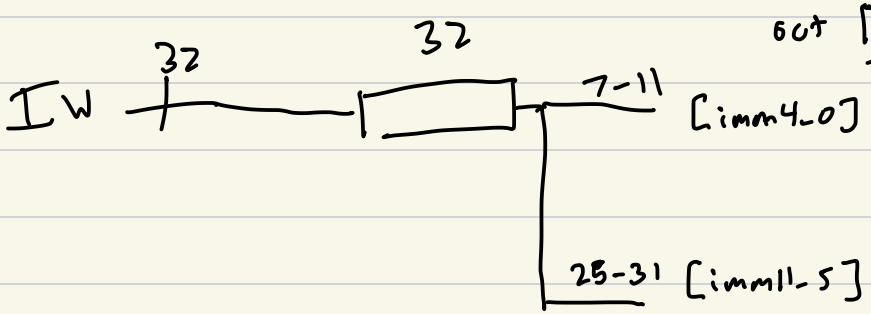
RR0 RR1

Imm Decoder

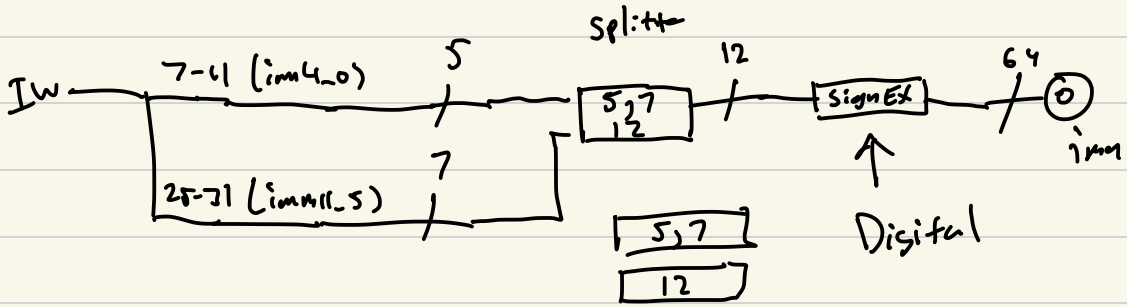


S type

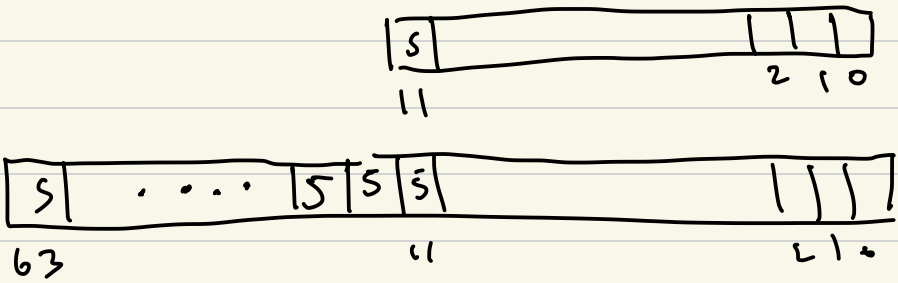
Splitter
in 32
out 7-11, 25-31

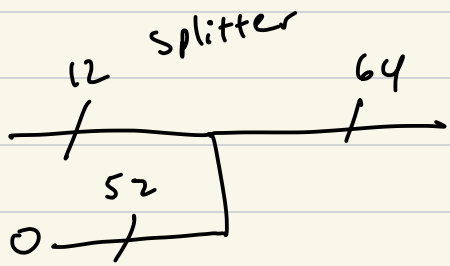


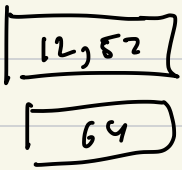
Goal 64 bit sign extended value

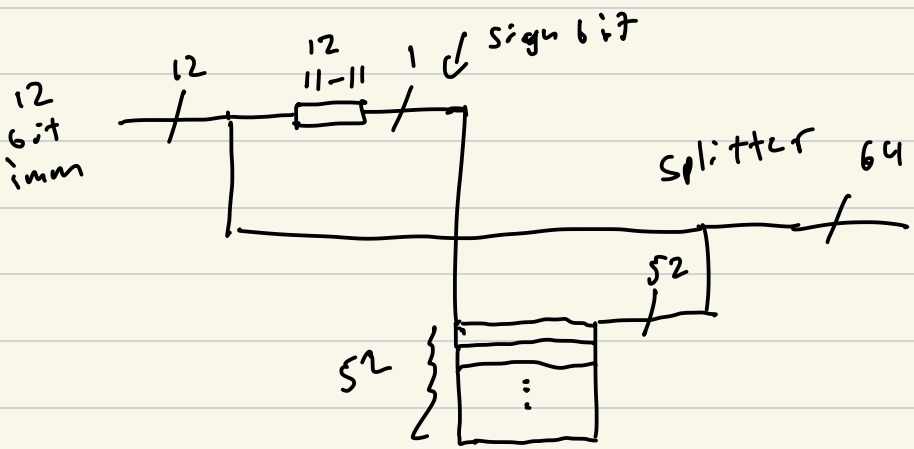


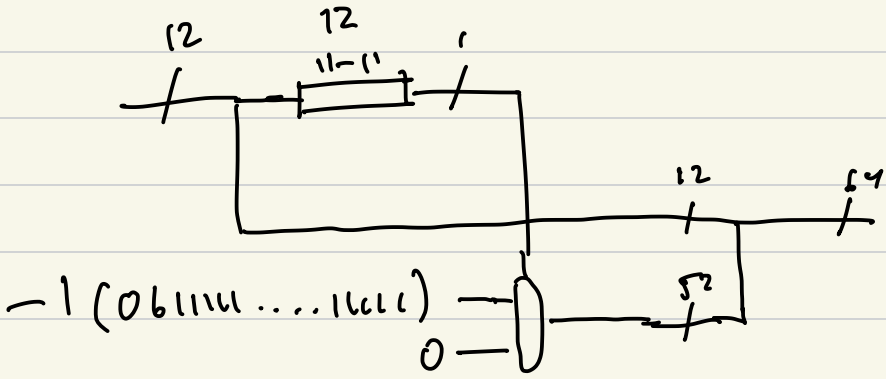
How to implement sign extender with a splitter










12
12
11-11
1
12
64
-1 (0111111....1111111)
0
32